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Design, Implementation and Performance Analysis of Low Power, Low Energy Adder Using Adibatic Logic in 45nm CMOS Sub-micron Technology

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***Abstract* — In this paper I had implemented the different two types of 1-bit adder using adiabatic logic and conventional CMOS logic in 45nm technology with LT spice. As we know Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc. we have compared the complementary pass transistor (CPL) logic and 2 phase clocked adiabatic static CMOS logic (2PASCL) 1-bit adder for power dissipation as well as energy consumption, result suggest adiabatic method has low power and low energy consumption compared to complementary pass transistor logic.**

***Keywords* — Adibatic Logic, CPL, 2PASCL, DSP, CMOS, Low Power.**

I. INTRODUCTION

Power consumption and it's minimization is one of the primary concerns in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to high power dissipation and it can lead to reliability and IC packaging problems.

Adiabatic logic reduces the energy dissipation by reducing the dissipation across resistances of conducting MOSFETs and recovering the part of energy given to the output back to the source, which extends the battery life. Several adiabatic logic styles are available but here we implemented two styles are 1n-1p Quasi adiabatic logic and 1n-1n Split level adiabatic logic. As we know Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. Apart from the basic addition adders also used in performing useful operations such as subtraction, multiplication, division, address calculation, etc.

II. ADIABATIC CHARGING VCS. CONVENTIONAL CHARGING

A. Conventional Charging

The dominant factor of power dissipation in a conventional CMOS device is the dynamic power required to charge and discharge the capacitive nodes within the circuit itself. To charge the node capacitance CL from a dc supply of potential VDD, an energy

$$E = C_L . V_{DD}^2 \dots \dots \dots \dots (1)$$

Iswithdrawn fromsupply. Only half of thisenergy istemporarily stored in capacitor CL. The remaining

$$E = 0.5 C_L . V_{DD}^2 \dots \dots \dots \dots (2)$$

Is dissipated as heat in the on resistance of PMOS. When input becomes logic high, the NMOS turns on and energy stored on capacitor CL is discharged to the ground and dissipated as heat. Hence during a complete charge-discharge cycle, the energy

$$E = C_L . V_{DD}^2 \dots \dots \dots \dots (3)$$

Is withdrawn from power supply and is dissipated as heat. Half of this energy is dissipated during charging and half is dissipated during discharging.

B. Adiabatic Charging

In static CMOS logic, the abrupt application of supply voltage gives rise to high potential across the switching device. The energy dissipation during charging and discharging can be minimized to a great effect by ensuring that the potential across switching device is kept sufficiently small. Adiabatic charging may be achieved by charging the capacitor from a time varying source that starts at 0V. Thistime varying source rises towards V at a slow rate that ensures that potential across switching device is kept arbitrarily small. The adiabatic charging is shown in figure 1.

In fact the energy dissipated across the resistance, R is

$$E_{diss.} = I^2 . RT = \frac{RC}{T} . C . V_{DD}^2 \dots \dots \dots \dots (4)$$

From the above equation (4), we can see that if T >> RC, the energy dissipation during charging Ediss ≈ 0. Same is applicable during discharge process. In addition to this, in some adiabatic logics, the energy dissipation also occurs due to threshold voltage of MOSFET and diode cut-in voltage. The energy dissipation due to threshold voltage Vt is

$$E = 0.5\, C . C_{vt}^2 \dots \dots \dots \dots (5)$$

The energy dissipation due to diode cut-in voltage Vd is

$$E = C_L . V_d . V_s \dots \dots \dots \dots (6)$$

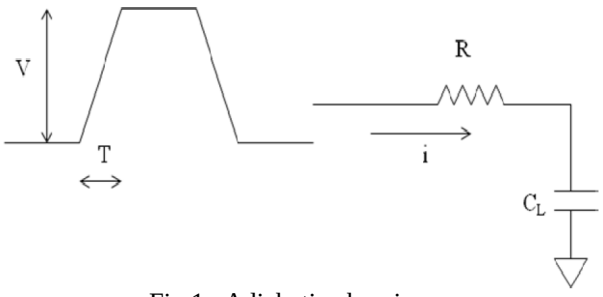

Fig.1. Adiabatic charging

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III. Design and Implementation of Adder

Different adiabatic logic styles contain different number of transistors and different number of power clocks. In this section we will study different adiabatic logic styles, which are derived from static CMOS, without large change: 2PASCL adiabatic logic and complementary pass transistor logic style are derived.

A. Two Phase Clocked Static CMOS Adiabatic Logic (2PASCL)

In the logic families which include diode in charging path suffer from output amplitude degradation. To deal with this problem, a new logic family named as two phase clocked adiabatic static CMOS logic. This logic family does not include diode in charging path, so that output amplitude degradation does not occur. The 2 phase clocked adiabatic static cmos logic uses a two phase clocking split level sinusoidal power supply. One is in phase while the other is inverted. The voltage level of Vclk exceeds that of Vclk by VDD/2. By using these two split – level sinusoidal waveforms, which have peak to peak voltages of 1V, the voltage difference between the current carrying electrodes can be minimized and subsequently, power consumption can be suppressed. It uses two diodes- one diode is placed between output node and power clock, Vclk and the other diode is placed adjacent to nmos logic circuit and connected to other power clock,Vclk . Both the diodes are used to recycle the charge from output node and to improve the discharging speed of internal nodes. Like other families discussed here, we have used MOSFET as diode by shorting gate and drain of mosfet together. The sources of power dissipation in this logic family are diode cut-in potential, threshold voltage of mosfet or the potential drop between drain and source of conducting MOSFETs and dissipation in resistance of pmos and nmos while charging and discharging the load. The use of slowly varying power clocks ensures the small energy dissipation across the ON resistance of MOS devices.The schematics to realize the Carry and Sum functions of a full adder using 2PASCL are shown in figure 3, figure 4 shows output waveforms.

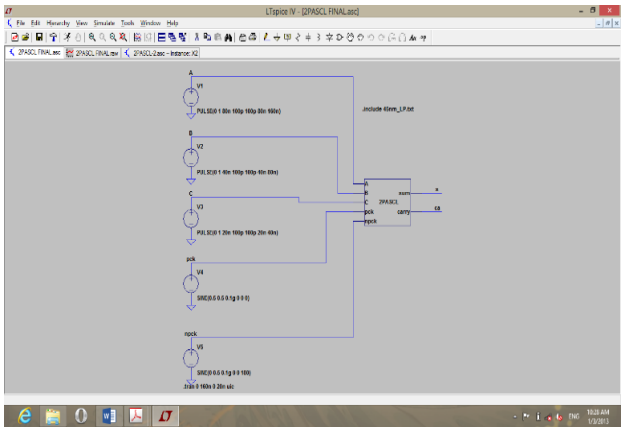

Fig. 2 Block diagram of 2PASCL.

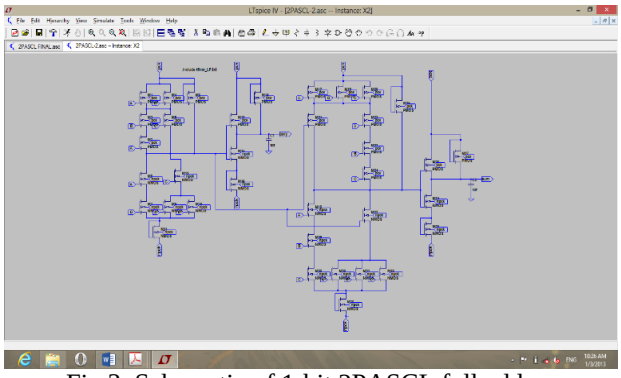

Fig.3. Schematic of 1-bit 2PASCL full adder.

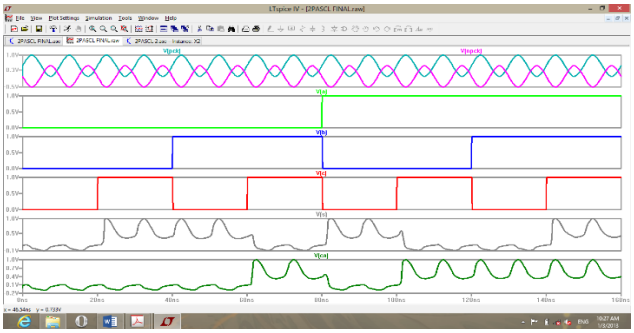

Fig.4. Simulation result of 1-bit 2PASCL full adder

B. Complementary Pass Transistor Full adder

The second style for full adder is conventional complementary pass transistor logic style in which carry and sum is implemented with inverted output. This technique generally used for high speed and low power compared to conventional static CMOS logic. The implementation of CPL 1-bit full adder shows in figure 6, where figure 7 shows simulation result of it.

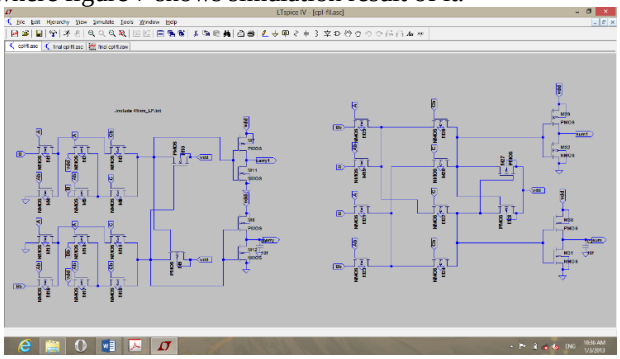

Fig.5. Block diagram of1 -bit CPL full adder

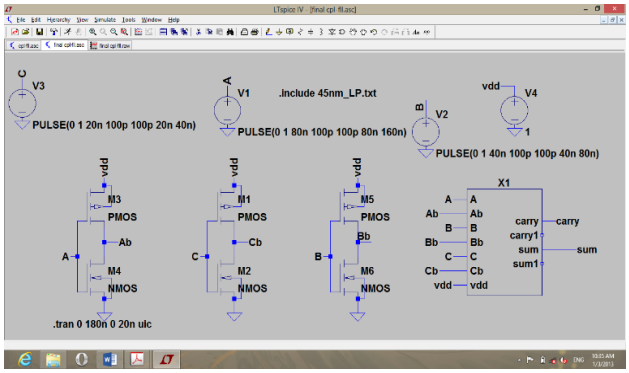

Fig.6. Schematic of 1-bit CPL full adder

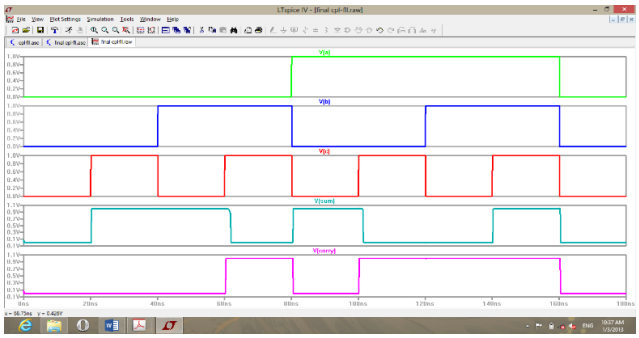

Fig.7. Simulation result of 1-bit 1n-1p CPL full adder

IV. Comparative Analysis of Adder

As we analysis all adder in 1-bit adder by varying the load capacitance start from 10fF to 200fF, by applying power clock of 100MHz, other inputs of 6.25MHz, 12.5MHz and 25MHz respectively, as we are increasing load capacitance dissipated power also increasing. By comparative analysis we can see that adiabatic logic has low power dissipation and low energy consumed compared to Complementary pass transistor logic.

Table I : Power Dissipation of 1-bit Full Adder

Load Capacitance (fF)	Average Energy Consumption (pJ)	
	2PASCL	CPL
10	0.7669	0.5008
20	0.8345	0.5526
30	0.1306	0.5959
40	0.1803	0.6826
50	0.2372	0.7506
60	0.2904	0.7517
70	0.3488	0.8372
80	0.3999	0.84
90	0.4533	0.9465
100	0.5088	0.9522
110	0.5685	1.0414
120	0.6276	1.0918
130	0.6877	1.0974
140	0.7465	1.1832
150	0.8158	1.2473
160	0.8761	1.2567
170	0.9451	1.3516
180	1.0106	1.3914
190	1.0711	1.3917
200	1.1379	1.439

Table II : Energy consumption of 1-bit full adder

Load Capacitance (fF)	Average Power Dissipation (uW)	
	2PASCL	CPL
10	0.4793	2.7825
20	0.5216	3.0702
30	0.8141	3.311
40	1.1274	3.7927
50	1.4826	4.1704
60	1.8154	4.1765
70	2.1803	4.6514
80	2.4996	4.6669
90	2.8334	5.2583
100	3.18	5.2903
110	3.5534	5.7853
120	3.9225	6.0657
130	4.2985	6.0964
140	4.6657	6.5734
150	5.0992	6.9296
160	5.4761	6.9816
170	5.9073	7.5087
180	6.3162	7.7299
190	6.6942	7.7316
200	7.1116	7.9945

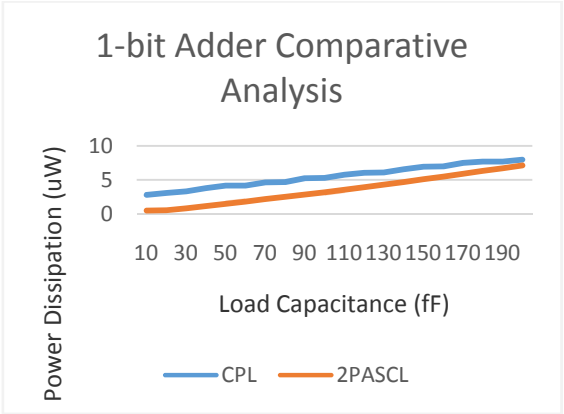

Fig.8. Graphical representation of 1-bit adder power dissipation

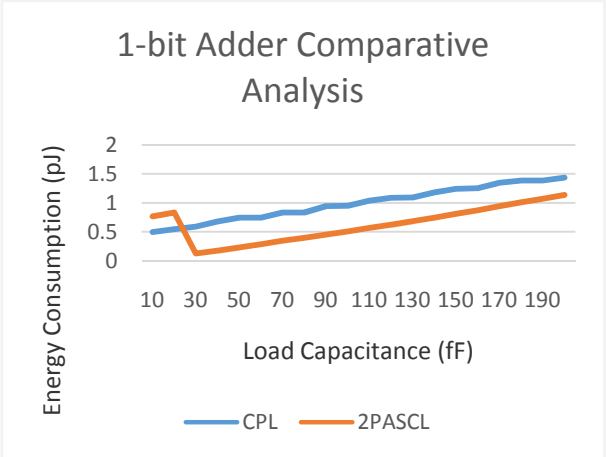

Fig.9. Graphical representation of 1-bit adder energy consumption

V. CONCLUSION

From all results display by graph and observed from the table 1 and table 2, we comes to know the adiabatic family has a low power dissipation as well as low power consumption compared to Complementary pass transistor adder. If we count the transistor number than adiabatic logic has high count having 35 transistor where complementary pass transistor logic has low transistor count having 32, than also we got low power and energy consumption in adiabatic logic family.

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